UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,094	10/14/2003	Frantisek Sukup	ONS00511	5498

7590 12/06/2004

James J. Stipanuk
Semiconductor Components Industries, L.L.C.
Patent Administration Dept., MD/A700
P.O. Box 62890
Phoenix, AZ 85082-2890

EXAMINER	
ZWEIZIG, JEFFERY SHAWN	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 12/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,094	SUKUP ET AL.	
	Examiner	Art Unit	
	Jeffrey S. Zweizig	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8,9 and 12-20* is/are rejected.

7)☒ Claim(s) *2-7,10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/14/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 2 and 15-20 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The continuity of the resistor recited in claim 2 is not understood. The claim fails to clearly associate the resistor with the bias current or the control terminal of the output transistor.

It is not understood toward what the "output" is directed as recited in the claims. Referring to claim 15 and Fig. 1, as best understood, there is current output at 19 and a voltage output at 36. As best understood, the initial current passes through component 17, not current output 19. Thus it is not understood toward what "output" claim 15 refers. Or it is not understood toward what the "first output current" refers. Also, it is not understood toward what the "first value of the output voltage" refers. As best understood, the first current through component 17 is responsive to an initial voltage at the input 22, not the output voltage at voltage output 36.

As best understood, the "bias current" recited in claim 16 is directed toward the current through components 14, 13 & 17 and the "output transistor" is directed toward component 12. Again, if the output transistor 12 is disabled as recited in claim 16, there would be no current at current output 19.

Claims 17 and 18 appear to be directed toward the current through component 17. Component 17 is coupled to the voltage output 36, not the current output 19.

Claim 19 appears to conflict with claim 16 in that the first current now flows through output transistor 12 instead of components 13 and 17. The current through output transistor 12 would be different than the current through components 13 & 17 and the current would be delivered to a completely different output. Specifically, the current would go to output 19 instead of output 36.

The "coupling" action of claim 20 is not understood. As shown in Fig. 1, the output transistor 12 is always physically connected to J-FET transistor 14, which is always physically connected to the high voltage input 22. The bias current is not the result of "coupling" components together, the bias current is the result of applying a voltage to the high voltage input 22.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 8, 9 and 12-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Wong et al.(USPN 6,775,164).

Fig. 1 discloses a high voltage device 124/20, an input voltage (from 110), an output transistor 20 and a switch 42 as recited in claim 1. An initial bias voltage through 124 is shunted away from output transistor 20 by switch 42. After an initial output voltage is reached, output transistor 20 is turned ON, generating an output current through 124 greater than the bias current.

Claims 8 and 9 are anticipated for the reasons above.

Further shown in Fig. 2 is a comparator transistor 140 as recited in claim 12.

A reference voltage (ground) is applied via transistor 146 as recited in claim 13.

The output is coupled at node 46 to disable the output by operating output transistor 20 as recited in claim 14.

As best understood, the output voltage and current (DC+) is returned at node 46 to disable the output by operating transistor 20 as recited in claim 15.

5. As best understood, claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Tisinger et al (USPN 5,477,175).

Fig. 1 discloses an output current through 102, an output voltage at 112 and a voltage return 105 for disabling transistor 102 thereby disabling the output voltage at 112.

Conclusion

6. Claims 2-7, 10 and 11 are objected to as being dependent upon a rejected base claim, but may be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey S. Zweizig whose telephone number is (571) 272-1758. The examiner can normally be reached on Monday thru Thursday 6:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeffrey S. Zweizig
Primary Examiner
Art Unit 2816

JZ